UNITED STATES PATENT AND TRADEMARK OFFICE

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ART UNIT	PAPER NUMBER
4113	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

PTOL-90A (Rev. 04/07)

	Application No.	Applicant(s)
Office Action Summary	10/573,566	OHTSUKA, TAKESHI
	Examiner	Art Unit
	Mark A. Giardino	~~2100~~ 4113

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL.**   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

     4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 March 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

     a)☒ All   b)☐ Some *   c)☐ None of:

       1.☐ Certified copies of the priority documents have been received.

       2.☐ Certified copies of the priority documents have been received in Application No. _____ .

       3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

     * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *3/27/2006*.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application

6) ☐ Other: _____ .

Claim Objections

Claim 12 is objected to because of the following informalities: The drive device

from Claim 11 is claimed, but there is no mention of this drive device in Claim 11 in the

preamble. The claim has been construed as if a computer program has been claimed in

the preamble. Appropriate correction is required.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of
matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the
conditions and requirements of this title.

Claims 10-12 are rejected under 35 U.S.C. 101 because the claimed invention is

directed to non-statutory subject matter. They claim a computer program, but this

program must be stored on a computer readable medium in order to be patentable.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that

form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public
use or on sale in this country, more than one year prior to the date of application for patent in the United
States.

Claims 1-3 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by

Ellis et al (US 6,029,226).

Regarding Claim 1, Ellis ('226) teaches a drive device for writing data transmitted by a host device onto a memory card in accordance with a command issued by the host device, comprising:

a receiving unit operable to receive a plurality of commands issued by the host device (see Column 3 Lines 24 and 28, where commands are received); and

a writing unit operable, if a write end address of one of the received commands is consecutive with a write start address of a following command, to perform the data writing to the memory card by the consecutive commands in a single process (see Column 6 Line 63 to Column 7 Line 5).

Regarding Claim 2, Ellis ('226) teaches all limitations of Claim 1, wherein

the process involves processing to sequentially write data received from the host device to the memory card being repeated until a STOP instruction is given (see Column 3 Lines 37-40, also a status field that indicates a transfer has finished Column 5 Lines 54-58), and the device further comprises:

an analysis unit operable to decode the write-start address and a sector number of each command, the sector number being the number of sectors of data for writing the command (such a unit is inherently present to load the buffer described in Column 5 Lines 33-37); and

an instruction unit operable to give the STOP instruction at a point when a written sector number reaches $s + t$, where s is the sector number of the one command and t is the sector number of the following command ($s + t$ sectors must be written for the consecutive write described in Column 6 Lines 17-25).

Regarding Claim 3, Ellis ('226) teaches all limitations of Claim 2, wherein the process is activated when the analysis unit decodes a write-start.address A and the sector number s from the one command, and involves the data writing being started from the write-start address A (see how the unit starts a write as soon as it receives address information, Column 6 Lines 6-12),

the analysis unit analyzes the following command until the sector number reaches s (see Column 6 Lines 17-22), and

the instruction unit gives the STOP instruction when the written sector number reaches $s + t$, if a write-start address B of the following command is consecutive with a write-end address $A + s$ of the one command (see Column 6 Lines 25-26 how both writes are treated as a single command and thus must have only one STOP instruction).

Regarding Claim 6, Ellis ('226) teaches all limitations of Claim 2, wherein a wait flag is appended to a command received from the host device, and if the command with the wait flag is received and a following command has yet to be received, the analysis and instruction units wait for the following command to be received (Column 5 Lines 54-58).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Ellis ('226) in view of Ellis et al (US 7,181,548).

Regarding Claim 4, all limitations of Claim 3 are discussed above. Ellis ('226)

teaches that tags may be appended to instructions (Column 5 Lines 1-8 in Ellis ('226)),

but does not specifically teach a prohibit flag appended to the one command that makes

the unit give a STOP instruction at a point when the written sector number reaches s if

the prohibit flag is appended to the one command. However, Ellis ('548) teaches a

'CqeNaca' bit and 'Naca' bit (Column 10 Lines 42-46), together which may be

considered a prohibit flag. When this flag is set, the next command will be treated as

sequential as described by Ellis ('226) (Column 6 Lines 16-26 in Ellis ('226)). Note that

Ellis ('226) teaches that the write-start address B of the following command must be

within $A + s$ of the following command and hence includes the case where B is

consecutive with $A + s$. If this flag is not enabled, the command will be treated as non-

sequential (Column 10 Lines 44-47 in Ellis ('548)) and thus fall under the first mode of

operation as described by Ellis ('226) (Column 6 Lines 6-12 in Ellis ('226)). It would

have been obvious to a person having ordinary skill in the art at the time the invention

was made to which the subject matter pertains to have used such a bit, since it is

partially described by Ellis ('226) when he describes managing sequences (Column 5

Lines 1-8). As motivation, if this flag is present and set, the memory device is freed

from having to check for a consecutive write address itself and thus makes the write

process faster. Thus, by using this flag, we obtain the additional benefit of improved

write performance, as would have been well known to one of ordinary skill in the art.

Regarding Claim 5, all limitations of Claim 3 are discussed above. Ellis ('226)

teaches tags that may be appended to instructions (Column 5 Lines 1-8 in Ellis ('226)),

but does not specifically teach a prohibit flag appended to the following command that

makes the unit give a STOP instruction at a point when the written sector number

reaches s if the prohibit flag is appended to the following command. However, Ellis

('548) teaches an "Enable Sequential" bit (Column 10 Lines 30-34 in Ellis ('548)), which

is a logically inverted prohibit flag. When this bit is set, the next command will be

treated as sequential as described by Ellis ('226) (Column 6 Lines 16-26 in Ellis ('226)).

If this Enable Sequential bit is not enabled, the commands are not treated as sequential

and thus fall under the first mode of operation as described by Ellis ('226) (Column 6

Lines 6-12 in Ellis ('226)). It would have been obvious to a person having ordinary skill

in the art at the time the invention was made to which the subject matter pertains to

have used such a bit, since it is partially described by Ellis ('226) when he describes

managing sequences (Column 5 Lines 1-8 in Ellis ('226)). Motivation is the same as

applied to Claim 4 above.

Claims 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis

('226) in view of Krantz (US 6,826,650).

Regarding Claims 7 and 8, Ellis ('226) teaches all limitations of Claim 3 as

discussed above, but does not teach a tag attached thereto, with the flags showing an

order of the commands. However, Krantz teaches a tag showing an order of the

commands (see address registers and description Column 2 Lines 18-36 in Krantz). He

also teaches a storage unit operable to store commands received from the host device

(buffer memory controller 230, also see Figure 1 in Krantz), a rearranging unit operable

to rearrange the stored commands in order of the write-start addresses (such a unit is

inherently present for the functionality described in Column 2 Lines 37-39 in Krantz)

wherein the analysis unit performs the analysis in the rearranged order of the

commands (such functionality is inherently present in the analysis unit for writing data

on consecutive tracks as described in Column 2 Lines 33-36). It would have been

obvious to a person having ordinary skill in the art at the time the invention was made to

which the subject matter pertains to have provided the extra hardware functionality as

listed above. Krantz provides the motivation when he states that adding these devices

improves system performance (Column 2 Lines 41-52 in Krantz).

Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Ellis ('226) in view of Carman et al (US 6,272,632).

Regarding Claim 10, Ellis ('226) teaches receiving a plurality of commands

issued by the host device (see Column 3 Lines 24 and 28 in Ellis ('226)); and if a write

end address of one of the received commands is consecutive with a write start address

of a following command, performing the data writing to the memory card by the

consecutive commands in a single process (see Column 6 Lines 63-67 to Column 7

Lines 1-5 in Ellis ('226)). However, Ellis ('226) teaches this functionality implemented in

hardware. Carman teaches advantages of using software instead of hardware (Column

1 Line 53 to Column 2 Line 7 in Carman). It would have been obvious to a person of

ordinary skill in the art at the time the invention was made to which the subject matter

pertains to have implemented the device described by Ellis ('226) in software. As

motivation, Carman lists the benefits of cost and ease of integration of software

compared to hardware (Column 1 Line 53 to Column 2 Line 7 in Carman). Thus, by

implementing the functionality in software, additional benefits are obtained.

Regarding Claim 11, all limitations of Claim 10 are addressed above, and the

combined device further teaches a computer program wherein

the process involves processing to sequentially write data received from the host

device to the memory card being repeated until a STOP instruction is given (see

Column 3 Lines 37-40, also a status field that indicates a transfer has finished Column 5

Lines 54-58 in Ellis ('226)), and the device further comprises:

the computer program causes the computer to perform the further steps of:

decoding the write-start address and a sector number of each command, the

sector number being the number of sectors of data for writing with the command (such

functionality must be present to load the buffer described in Column 5 Lines 33-37 in

Ellis ('226)); and

giving the STOP instruction at a point when a written sector number reaches $s +$

t where s is the sector number of one command t is the sector number of the following

command ($s + t$ sectors must be written for the consecutive write described in Column 6

Lines 17-25 in Ellis ('226)).

Regarding Claim 12, all limitations of Claim 11 are addressed above, and the

combined device further teaches a computer program wherein

the process is activated when a write-start address A and the sector number s

from the one command is decoded, and involves the data writing being started from the

write-start address A (see how the unit starts a write as soon as it receives address and

other information, Column 6 Lines 6-12 in Ellis ('226)),

the following command is analyzed until the written sector number reaches s,

and (see Column 6 Lines 17-22 in Ellis ('226)), and

the STOP instruction is given when the written sector number reaches $s + t$, if a

write-start address B of the following command is consecutive with a write-end address

$A + s$ of the one command (see Column 6 Lines 25-26 in Ellis ('226) how both writes are

treated as a single command and thus must have only one STOP instruction).

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ellis

('226) in view of Harari et al (US 5,297,148).

All limitations of Claim 2 have been discussed above. However, Ellis ('226) does

not teach an analysis unit that judges if the number of sectors is an integer multiple of

the number of sectors in an erasable block of the memory card, and if the unit is judged

in the negative, the instruction unit continues the process by not giving the STOP

instruction even if the written sector number reaches $s + t$, and waits for a further

command to be received. However, Oyaizu teaches a flash memory buffer that holds

bytes of write information until it is ready to be written to a flash memory device (see

Column 14 Line 41 to Column 15 Line 16 in Harari). It would have been obvious to a

person of ordinary skill in the art at the time the invention was made to have stored the

write information in a buffer and wait until an integer multiple of the number of sectors were stored before acknowledging the STOP instruction from the host. As motivation, memory blocks are erased in block units and cannot be re-written without re-writing the entire contents of the block (see Column 4 Lines 44-49 in Harari). Therefore, a person having ordinary skill in the art would want to make sure that before writing to a block, as much data as possible is ready to be written to said block to avoid re-writing the block several times sequentially, thereby causing delays in write times. So, by combining the two devices, the additional benefit of faster write times is obtained.

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Rosich et al (US 5,551,002) teach a way of merging consecutive writes. Konishi et al (US 5,570,002) teach a buffer for storing write data between an EEPROM and a host device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark A. Giardino whose telephone number is (571) 270-3565. The examiner can normally be reached on M-R 7:30 - 5:00. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Robertson can be reached at (571) 272-4186. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.
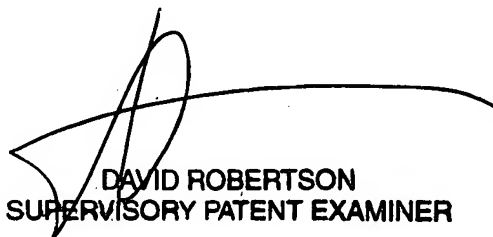
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USPTO Customer Service Representative or access to the automated information

system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

M.A. Giardino

9/6/2007

DAVID ROBERTSON
SUPERVISORY PATENT EXAMINER